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Title of Invention: **RECEIVER OF DIGITAL SIGNALS HAVING A VARIABLE HYSTERESIS, IN PARTICULAR FOR AUDIO DIGITAL APPLICATION**

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- Utility Application Transmittal
- Specification and Claims (23 pages)
- Drawings (5 pages)
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RECEIVER OF DIGITAL SIGNALS HAVING A VARIABLE HYSTERESIS, IN PARTICULAR FOR AUDIO DIGITAL APPLICATION

PRIORITY CLAIM

[1] This application claims priority from European patent application No. 02425804.8, filed December 30, 2002, which is incorporated herein by reference.

TECHNICAL FIELD

[2] The present invention relates to a receiver of digital signals originated from very different sources.

[3] In particular, the receiver according to an embodiment of the invention is capable of supporting input signals of the single-ended type (for consumer applications) or of the differential type (for professional applications), with extremely variable voltage ranges (even higher than a supply voltage) and possibly affected by noises, generally indicated in the following description as ALL-INPUT signals.

[4] More specifically, an embodiment of the invention relates to a receiver of ALL-INPUT signals comprising a conversion stage of the ALL-INPUT/single-ended type inserted between a supply voltage reference and a ground and having a first and a second input terminal effective to receive digital signals, an output terminal effective to provide an analog signal and a bias terminal effective to receive a bias current, as well as an hysteresis comparator.

[5] Embodiments of the invention relate particularly, but not exclusively, to a receiver of digital audio signals and the following description is made with reference to this field of application for convenience of illustration only.

BACKGROUND

[6] As it is well known, in the field of digital audio applications, data affected by noise originated from an optical fibre (POF) or a coaxial cable must be

reconstructed. Data can be single-end or differential. To this purpose it is possible to use hysteresis comparators or Schmitt triggers, well known in the prior art.

[7] By way of example, **FIG. 1** shows a single-end hysteresis comparator 10 essentially comprising a positive-feedback operational amplifier 11.

[8] In particular, the operational amplifier 11 has an inverting input terminal (-) receiving an input voltage signal Vi and an output terminal being feedback-connected, by means of a resistor R2, to a non-inverting input terminal (+) and effective to provide an output voltage signal Vo.

[9] The non-inverting input terminal (+) is also connected to a voltage reference –Vdd by means of a further resistor R1. A voltage value V+ is then provided to this non-inverting input terminal (+), being equal to:

$$V+ = \beta V_0 \qquad (1)$$

being:

V_0 the voltage value on the output terminal of the operational amplifier 11;

β a feedback coefficient equal to $R_1/(R_1+R_2)$.

[10] It is also possible to optimize such an hysteresis comparator by means of a MOS configuration, schematically shown in **FIG. 2** and globally indicated with 20. In particular the hysteresis comparator 20 is inserted between a supply voltage reference Vplus and a ground Vminus and it comprises a single-ended-configured Schmitt trigger 21 being cascade-connected to a buffer 22 between an input terminal IN and an output terminal TRIGGER.

[11] In particular, the Schmitt trigger 21 comprises:

a first pair of PMOS transistors, M13 and M14, inserted, in series to each other, between the supply voltage reference Vplus and an inner circuit node triggNEG and having the control terminals connected to each other and to the input terminal IN of the hysteresis comparator 20;

a second pair of NMOS transistors, M17 and M18, inserted, in series to each other, between the inner circuit node triggNEG and the ground Vminus and having the control terminals connected to each other and to the input terminal IN of the

hysteresis comparator 20;

a further PMOS transistor M12 inserted between an intermediate node X21 between the transistors M13 and M14 of the first pair of PMOS transistors and the ground Vminus; and

a further NMOS transistor M19 inserted between the supply voltage reference Vplus and an intermediate node X22 between the transistors M17 and M18 of the second pair of NMOS transistors.

[12] Transistors M12 and M19 have respective control terminals connected to each other and to the inner circuit node triggNEG, as well as to the buffer 22.

[13] In particular, the buffer 22 comprises a first M11 and a second M20 transistor, respectively of the PMOS and NMOS type, connected, in series to each other, between the supply voltage reference Vplus and the ground Vminus, and having the control terminals connected to the control terminals of the transistors M12 and M19 of the Schmitt trigger 21.

[14] Finally, transistors M11 and M20 are connected to each other in correspondence of the output terminal TRIGGER of the hysteresis comparator 20.

[15] The aim of known hysteresis comparators, whose transfer function is shown in **FIG. 3**, is essentially to avoid the comparison uncertainty when the input signal, with noise, crosses the switching threshold.

[16] In particular, in the example shown in **FIGS. 4 and 5**, a input signal being monotonic at intervals is considered, to which a white noise having a predetermined variance is added. The additional white noise causes a repeated zero-crossing of the signal received by the hysteresis-free comparator generating a series of undesired switchings at the comparator output. These undesired switchings are removed by means of a traditional hysteresis comparator (as shown in **FIGS. 1 and 2**).

[17] Moreover, although advantageous under several aspects, known solutions have technological limitations penalizing the industry cost, for example not allowing the CMOS technology implementation thereof.

[18] Moreover, as in the case of a traditional hysteresis comparator 20, it happens that, even though the comparator has good features in terms of speed, power consumption and noise rejection, it does not satisfy the following specifications generally required by the different applications:

it does not allow a signal with broad dynamics, for example from 200 mV to 10 Volts, to be directly interfaced by using a receiver implemented with a low supply voltage technology (<2.5V);

it is not compatible with the standards requiring different hysteresis values;

it does not reach a sufficiently high response speed with a reduced power consumption required by portable battery applications if an operational amplifier is used (such as for example in the configuration shown in **FIG. 1**);

it is not compatible with single-ended/differential input signals without performance lost.

[19] The problems linked to the low supply voltages (traditionally <2.5V, but also 1.8V), as well as to the use of the devices in extremely variable voltage ranges, as well as with noise, are essentially unsolved.

[20] In other words, the need for devices being capable of supporting ALL-INPUT signals, i.e. input signals of the single-ended type (for consumer applications) and of the differential type (for professional applications), is increasingly felt, with extremely variable voltage ranges (even higher than a supply voltage) and possibly affected by noises.

[21] A technical problem underlying embodiments of the present invention is to provide an hysteresis comparator which can be integrated in low-cost technologies without external components, capable of reconstructing a datum originated from an ALL-INPUT signal in a "free" digital signal (and thus usable for example in DSP applications), having such structural and functional features as to overcome the limitations still affecting prior art devices.

SUMMARY

[22] An idea underlying an aspect of the present invention is to perform, before sending the signals to the hysteresis comparator, an ALL-INPUT/single-ended conversion.

[23] Based on this idea the technical problem is solved according to one aspect of the present invention by a receiver essentially comprising a converter from an ALL-INPUT signal to an intermediate signal, for example of the trapezoidal type, as well as a traditional hysteresis comparator (comprising for example a Schmitt trigger). Advantageously according to an aspect of the invention, operating on the intermediate signal slope, together with the fixed comparison thresholds of the hysteresis comparator, the receiver operates as a variable-threshold hysteresis comparator.

[24] More particularly, the technical problem is solved according to another aspect of the present invention by a signal receiver inserted between a first and a second voltage reference and having a first and a second input terminal effective to receive differential signals and an output terminal effective to provide a converted signal, characterized in that it comprises a conversion stage inserted between said first and second voltage references and connected between said first and second input terminals of said signal receiver and an input terminal of an hysteresis comparator, connected in turn to said output terminal of said signal receiver, said conversion stage performing a conversion from any input signal received on respective input terminals to an intermediate signal provided on an output terminal and suitable for reception by said hysteresis comparator.

[25] The features and advantages of the receiver according to embodiments of the invention will be apparent from the following description of embodiments thereof given by way of non-limiting example with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[26] **FIG. 1** schematically shows a prior art hysteresis comparator;

[27] **FIG. 2** schematically shows an alternative embodiment of a prior art hysteresis comparator;

[28] **FIG. 3** shows the transfer function of a prior art hysteresis comparator;

[29] **FIG. 4** shows the evolution in time of signals in a prior art hysteresis comparator;

[30] **FIG. 5** shows the evolution in time of the input and output signals of an hysteresis-free comparator with and without noise superimposed to the input;

[31] **FIG. 6** schematically shows an ALL-INPUT/single-ended conversion stage according to an embodiment of the invention;

[32] **FIG. 7** schematically shows a signal receiver according to an embodiment of the invention;

[33] **FIGS. 8 and 9** show the evolution in time of input (RXP, RXN) and intermediate output (VDIFSING) signals, as well as a final output signal (VTRIG) of the receiver of **FIG. 7**.

DETAILED DESCRIPTION

[34] The following discussion is presented to enable a person skilled in the art to make and use the invention. Various modifications to the embodiments will be readily apparent to those skilled in the art, and the generic principles herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[35] A variable hysteresis receiver of digital signals, particularly for digital audio applications, is described hereafter, schematically illustrated in **FIG. 7**, globally

indicated with 70. Advantageously according to an embodiment of the invention, the receiver 70 essentially comprises a conversion stage 60 from an ALL-INPUT signal to an intermediate signal, for example of the trapezoidal type, as well as a traditional hysteresis comparator 20.

[36] The output of such a digital receiver 70 is then to be processed by a digital signal processor (DSP) or however by a general microprocessor.

[37] **FIG. 6** shows an ALL-INPUT/single-ended conversion stage 60 according to an embodiment of the invention.

[38] The conversion stage 60 is inserted between a first voltage reference, particularly a supply voltage reference Vplus, and a second voltage reference, particularly a ground Vminus, and it has essentially a current-mode structure formed by a plurality of current mirrors formed by means of MOS transistors. The conversion stage 60 has a pair of input terminals A and B, an output terminal OUT and a bias terminal TP receiving a bias current Ipolar.

[39] In greater detail, the conversion stage 60 comprises a first current mirror 61 connected to the supply voltage reference Vplus and to the input terminals A and B, as well as to the bias terminal TP. The first current mirror 61 comprises a first M1, a second M2 and a third M3 P-channel MOS transistor.

[40] The first transistor M1 is inserted between the supply voltage reference Vplus and the first input terminal A, to which it is connected by means of a first R1 and a second R2 resistor, and it has a control terminal connected to the control terminal of the second M2 and third M3 transistor.

[41] The second diode-configured transistor M2 is inserted between the supply voltage reference Vplus and the bias terminal TP and it has a control terminal connected to the control terminal of the first transistor M1 and to the bias terminal TP.

[42] The third transistor M3 is inserted between the supply voltage reference Vplus and the second input terminal B, to which it is connected by means of a third R3 and a fourth R4 resistor, and it has a control terminal connected to the control

terminal of the first M1 and second M2 transistor.

[43] The conversion stage 60 comprises also a second current mirror 62 connected to the ground Vminus and to the first input terminal A, as well as to a circuit node X. The second current mirror 62 comprises a fourth M4 and a fifth M5 N-channel MOS transistor.

[44] In particular, the fourth diode-configured transistor M4 is inserted between the first input terminal A, to which it is connected by means of a fifth resistor R5 and the second resistor R2, and the ground Vminus and it has a control terminal connected to the control terminal of the fifth transistor M5.

[45] The fifth transistor M5 is inserted between the circuit node X and the ground Vminus and it has a control terminal connected to the control terminal of the fourth transistor M4.

[46] The conversion stage 60 further comprises a third current mirror 63 connected to the ground Vminus and to the second input terminal B, as well as to the output terminal OUT. The third current mirror 63 comprises a sixth M6 and a seventh M7 N-channel MOS transistor.

[47] In particular, the sixth diode-configured transistor M6 is inserted between the second input terminal B, to which it is connected by means of a sixth resistor R6 and the fourth resistor R4, and the ground Vminus and it has a control terminal connected to the control terminal of the seventh transistor M7.

[48] The seventh transistor M7 is inserted between the output terminal OUT and the ground Vminus and it has a control terminal connected to the control terminal of the sixth transistor M6.

[49] The conversion stage 60 finally comprises a fourth current mirror 64 connected to the supply voltage reference Vplus, to the circuit node X, as well as to the output terminal OUT. The fourth current mirror 64 comprises an eighth M8 and a ninth M9 P-channel MOS transistor.

[50] In particular, the eighth diode-configured transistor M8 is inserted between

the supply voltage reference Vplus and the circuit node X and it has a control terminal connected to the control terminal of the ninth transistor M9.

[51] The ninth transistor M9 is inserted between the supply voltage reference Vplus and the output terminal OUT and it has a control terminal connected to the control terminal of the eighth transistor M8.

[52] The first A and second B input terminals are connected to each other by means of a further seventh resistor R7.

[53] Finally, the conversion stage 60 comprises a current-voltage converter 65, inserted between the supply voltage reference Vplus and the ground Vminus and connected to the output terminal OUT of the conversion stage 60.

[54] In particular, the current-voltage converter 65 comprises a tenth MOS transistor M10 inserted between the supply voltage reference Vplus and the output terminal OUT of the conversion stage 60, in parallel with the ninth transistor M9 comprised in the fourth current mirror 64, and having a control terminal connected to the output terminal OUT.

[55] The current-voltage converter 65 also comprises an eleventh MOS transistor M11 inserted between the output terminal OUT and the ground Vminus, in parallel with the seventh transistor M7 comprised in the third current mirror 63 and having a control terminal connected to the output terminal OUT.

[56] In the example shown, transistors M10 and M11 are P-channel and N-channel respectively.

[57] It is worth noting that resistors R1, R2, R3, R4, R5, R6 and R7 form a resistive bridge 66 adjusting the impedance of the conversion stage 60 with the impedance of a possible coaxial cable connected to the input terminals A and B and it protects the transistors comprised in the stage 60 from an excessive overvoltage.

[58] Advantageously according to an embodiment of the invention, it is possible to implement the conversion stage 60 in a low supply voltage technology (i.e. for

supply voltage values being lower than 2.5V) and to interface it directly to a signal originated from a coaxial cable, whose dynamics can reach 10 volts for some standards.

[59] The operation of the conversion stage 60 according to the described embodiment of the invention will now be described.

[60] One feature consists in keeping the impedance detected at each node thereof at a value equal to 1/gm, succeeding therefore in being intrinsically fast also for low bias currents. The feedback lack makes the conversion stage 60 according to the described embodiment of the invention unconditionally stable when the bias current Ipolar varies. Traditionally all mirrors have a unitary multiplication factor except for mirrors 62 and 63 which can have a factor different from one, but equal for both, according to design specifications.

[61] It is worth noting that this bias current Ipolar actually determines the stage gain and, in fact, the dynamics of the hysteresis voltage thereof.

[62] Finally, the current-voltage converter 65 determines the stage 60 gain.

[63] In fact, the input voltage RXP-RXN is converted into current in the resistive input network mirrored on the output stage 65 wherein it is converted again into voltage. The output/input gain is directly proportional to the resistance value detected at the output node of the stage 60, i.e. Rout = 1/[Rds9//Rds7//(1/gm10)//(1/gm11)].

[64] In practice, being Rds9 and Rds7 >> 1/gm10 and 1/gm 11, Rout is fixed at first approximation by the transconductance of MOS transistors M10 and M11. By varying these transconductances, it is thus possible to change the slope of the edges of the signal V(DIFSING), as shown in **FIGS. 8 and 9**, varying thus also the overall receiver hysteresis.

[65] The output terminal OUT thus comprises a still analog converted signal of the single-end type V(DIFSING) capable of driving an inverting hysteresis comparator, such as the Schmitt trigger described with reference to the prior art and schematically shown in **FIG. 2**.

[66] Moreover the input block of the stage 60, composed of the resistive network 66, the current IPOLAR and MOS transistors M1, M3, M4, M6, self-biases input nodes A and B at a reference voltage comprised between Vplus and Vminus, providing the greatest versatility of use, with any source (single-ended or differential).

[67] A variable hysteresis receiver 70 of digital signals according to an embodiment of the invention, as schematically shown in **FIG. 7**, is thus obtained.

[68] In particular, the hysteresis comparator 70 comprises a conversion stage 60 inserted between the supply voltage reference Vplus and the ground Vminus and having the bias terminal TP connected to a generator GP of the bias current Ipolar, as well as the output terminal OUT connected to the input terminal IN of an hysteresis comparator 20, in particular a Schmitt trigger, inserted in turn between the supply voltage reference Vplus and the ground Vminus and having an output terminal TRIGGER effective to provide a "free" output signal.

[69] It must be remembered that the Schmitt trigger 20 has an hysteresis cycle equal to:

$$Vhys = (Vplus\text{-}Vminus) - (\Delta V_N\text{-}\Delta V_P) \quad (2)$$

Being:

Vhys the hysteresis voltage of the Schmitt trigger 20;

Vplus the positive supply voltage of the Schmitt trigger 20; and

Vminus the negative supply voltage of the Schmitt trigger 20 (traditionally the ground)

$$\Delta V_N = |Vth19\text{-}Vth18| \quad (3)$$

$$\Delta V_P = |Vth12\text{-}Vth13| \quad (4)$$

where Vth19, Vth18, Vth12 and Vth13 are the threshold voltages of transistors M19, M18, M12 and M13 respectively, comprised in the Schmitt trigger 20, as shown in **FIG. 2**.

[70] It is thus possible to change the hysteresis voltage operating on the geometries of these transistors M18, M19, M12 and M13 comprised in the Schmitt

trigger 20 in order to change the transistor threshold voltages Vth according to the relations (3) and (4) and thus to change the hysteresis voltage according to the relation (2).

[71] In particular, the conversion stage 60 allows a differential single-ended converter to be manufactured, by means of a CMOS architecture, to be performed, wherein the geometries of the transistors used determine the hysteresis voltage for an allotted bias current. The conversion stage similarly allows the hysteresis voltage and the operating band to be dynamically changed in time when the bias current changes.

[72] Advantageously according to the described embodiment of the invention, in order to limit the range of possibilities being theoretically obtainable, it is easy to set the hysteresis voltage by changing the geometries of the transistors M10 and M11 comprised in the current-voltage converter 65 of the conversion stage 60. It is also possible to set the hysteresis voltage by changing the bias current Ipolar.

[73] The hysteresis comparator 70 obtained from the cascade-connected conversion stage 60 according to the described embodiment of the invention and Schmitt trigger 20 is thus more versatile and flexible than a prior art hysteresis comparator.

[74] Advantageously according to the described embodiment of the invention, the hysteresis comparator 70 can be used as ALL-INPUT signal receiver.

[75] If the input signal is differential (such as in professional audio applications) both input terminals RXP and RXN are connected to the source. For convenience of illustrations, the input terminals of the receiver 70 and the signal thereon will be indifferently indicated with RXP and RXN.

[76] If the input signal is single-ended, it is sufficient to connect any of the two terminals RXP or RXN to the signal source, connecting the other terminal to ground.

[77] Capacitances C1 and C2, respectively connected between the terminals RXP, RXN of the variable hysteresis receiver of digital signals 70 and the input

terminals A, B of the stage 60, uncouple the receiver 70 from the source. The input of the stage 60 (A and B) self-biases itself to the correct bias voltage (as previously explained).

[78] The operation of the conversion stage 60 and of a signal receiver 70 according to the described embodiment of the invention has been simulated by the Applicant and tested under noisy signal conditions. The results being obtained are indicated in **FIGS. 8 and 9**.

[79] In particular, **FIG. 8** shows the evolution of a signal on the output terminal OUT of the conversion stage 60, indicated with V(DIFSING), for a differential input on the terminals RXP and RXN with a noise overlapped to RXP being higher than the dynamics of the signal (and ideal RXN).

[80] It can thus be seen how the reconstructed signal V(DIFSING) is correct, the noise having been correctly removed. The signal receiver 70 according to the described embodiment of the invention thus allows the signal on the output terminal TRIGGER of the Schmitt trigger 20, indicated with V(TRIG) in **FIG. 8**, to be optimally squared.

[81] **FIG. 9** shows the same signals with noise on both inputs RXP and RXN. It can be immediately noticed that the variable hysteresis receiver of digital signals 70 operates correctly even in this extreme condition.

[82] In other words, the variable hysteresis receiver of digital signals 70 according to the described embodiment of the invention allows a differential noisy signal to be correctly reconstructed.

[83] In conclusion, the conversion stage 60 and the hysteresis comparator 20 allow a receiver 70 of differential signals capable of operating correctly with noisy signals to be realized (even when noise exceeds the signal dynamics) and meanwhile they allow the following advantages to be achieved:

they allow the impedance to be adjusted with respect to the source (and/or cable), due to the resistive bridge (66) connected to the input terminals;

they allow the hysteresis voltage to be adjusted by changing the geometries

of the transistors (M10, M11) comprised therein or by varying the bias current (Ipolar); the hysteresis voltage can thus be fitted to the specifications imposed by different standards;

they have a high response speed even for low bias currents operating in current modes (current mirrors have a low impedance = 1/gm, being intrinsically fast);

they are stable when the bias current (Ipolar) varies due to the feedback lack; and

they can be implemented in a low supply voltage technology.

[84] Finally, advantageously according to embodiments of the invention, it is possible to realize a receiver of differential signals capable of operating at a high bit rate with a negligible power consumption, being thus suitable for portable battery applications.

[85] Essentially, advantageously according to embodiments of the invention, the receiver provided can be integrated in low-cost CMOS technologies, with low supply voltage (traditionally <2.5V, but also 1.8V) and it has a high possible versatility of use.

[86] Moreover, advantageously according to embodiments of the invention, the receiver provided is capable of supporting signals of the single-ended type (for consumer applications) or of the differential type (for professional applications).

[87] Finally, the receiver provided supports a range of extremely variable voltages (for example, in the case of S/PDIF standards transmissions of digital data in the range 200mV-7V are allowed), as well as signals affected by noises, for example mainly linked to the transmission means, being as much critical as the signal is low.

[88] In conclusion, the receiver according to embodiments of the invention supports ALL-INPUT input signals without using external resistive dividers or level-shifters.

[89] From the foregoing it will be appreciated that, although specific embodiments

of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention.